A Family of 2-20GHz Broadband Low Noise AlGaAs HEMT MMIC Amplifiers

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Abstract

Rapid advances in AlGaAs High Electron Mobility Transistor (HEMT) processing technology have made HEMT MMIC technology possible. This paper presents design and development information on a family of broadband, low noise amplifiers. Amplifiers covering the 2-20 GHz frequency band have been developed, and achieve noise figures comparable to their counterpart in hybrid HEMT technology. The amplifiers are configured in a cascadable design, with simultaneous low input and output VSWR, and flat gain response. Performance results include measured and modeled data for a 2-7 GHz LNA with 2.5 dB noise figure, a 2-20 GHz distributed amplifier with 9.5 dB flat gain, less than 3.5 dB noise figure, and a 5-11 GHz balanced LNA with 10dB gain, less than 2.5dB noise figure (6-11GHz) . Other octave band balanced amplifier designs are currently being fabricated (2-7GHz, 9-19GHz) and performance results are expected January '89. A preliminary temperature step-stress reliability evaluation on the discrete process HEMT device is also presented.

Introduction Design and process maturity in traditional GaAs MESFET technology, has provided impetus towards developing GaAlAs High Electron Mobility Transistor(HEMT) monolithic circuits. The superior noise figure capability of the HEMT as compared to the MESFET, makes the low noise amplifier an ideal candidate for HEMT MMIC development. The availability of such low-noise monolithic amplifiers allows applications in front-end electronics array applications, as well as in traditional EW applications.

This paper describes the technology development leading to a family of HEMT monolithic low noise amplifiers, and presents modeled and measured performance data on LNAs covering the 2-20 GHz frequency band. The measured noise figures are less than any reported data for HEMT (octave or decade band) MMIC low noise amplifiers [1] [4] [5] and compare favorably with hybrid HEMT LNAs.

Design Traditional amplifier design concepts have precluded analytical realizations of low noise amplifiers, due to the difficulty of achieving simultaneous low noise figure and good input VSWR, over the band of interest. Instead, low noise amplifier design has relied on exhaustive bench-tuning to empirically converge on the required performance. With the advent of GaAs MESFET MMIC technology tremendous strides have been made in realizing a variety of amplifier functions. However, the amplifiers have been generally developed as generic gain blocks, and have largely ignored the broadband low noise designs. This has thus precluded the receiver front-end from the benefits of monolithic technology, including size and weight reduction, broader bandwidth operation, and unit reproducibility. The lower noise AlGaAs HEMT device, when combined with the GaAs MMIC technology, can be now used to produce monolithic low noise amplifiers. This translates to tremendous capability advantages for space-borne receiver systems.

This paper presents design details on a family of HEMT low noise amplifiers covering the 2-20 GHz frequency band. Table 1 presents the band splits, and the noise figure and gain targets for each respective band. With such broad bandwidths, the likelihood of simultaneous low noise match with low input VSWR match is very low. Thus the designs are realized in a single ended or balanced topology, with multi-section Chebyshev noise matching circuits for optimum broadband performance[2], or a distributed topology for decade bandwidths.

The basic device noise parameters are measured on an in-house developed on-wafer RF test station using Cascade 50-ohm probes and ATN Inc. complex noise impedance analyzers. A representative plot of the 200 micron (4x50um interdigitated) device noise parameters and s-parameters are plotted in figure 1. Figure 2 shows the device small signal model at the low noise bias, extracted from the data in figure 1. The low Cgs and low (Rg+Ri) reflect the positive impact of the 0.2 micron 'T-Gate' structure described later in this paper. The minimum device noise figure for the initial design simulations was 0.6 dB at 12GHz with an associated transconductance of 315 mS/mm. This represented the available data as measured on a discrete process HEMT device[3].

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Table 1. **Multi-Stage Amplifier Performance Goals**

Freq (Ghz)	NF (dB)	Gain (dB)	IP3(dBm)	VSWR	TOPOLOGY
2-7	<1.5	30	>17	<1.5:1	Balanced
5-10	<2.0	30	>17	<1.5:1	Balanced
9-19	<3.0	30	>17	<2.0:1	Balanced
2-20	<3.0	30	>17	<1.5:1	Distributed

Figure 1. **200um MMIC PROCESS HEMT S11, S22, Γopt, 1-20GHz in 1GHz steps**

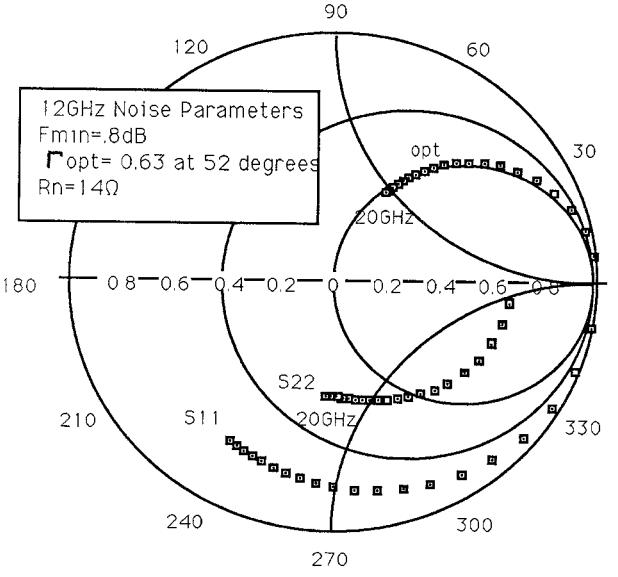
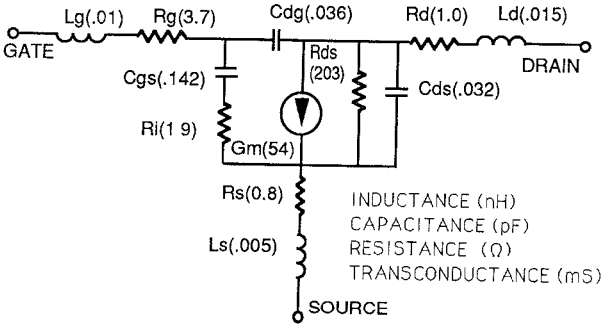


Figure 2. **200um HEMT Equivalent Circuit Model at Low Noise Bias (MMIC Process)**

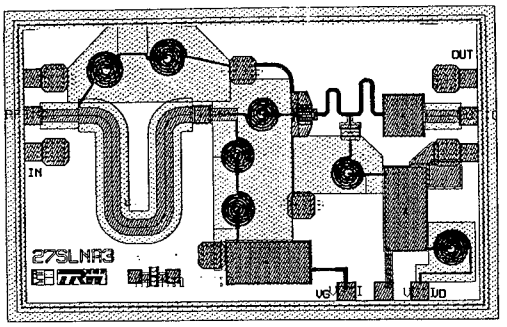


The balanced amplifier is readily suited for octave band designs, and provides design flexibility in achieving optimum noise match. The overall input/output VSWR is then determined by the 3-dB Lange coupler and the noise figure is degraded only by the insertion loss in the coupler. As part of this effort GaAs Lange coupler measurements have been made and have shown less than 0.6dB insertion loss at 12 GHz. Within the balanced topology the single ended input broadband noise matching circuits employ three section Chebyshev filters with impedance inverters[2] and series feedback to reduce the magnitude of S11 and gamma opt of the transistor. Two stage balanced amplifiers have been designed which utilize shunt feedback interstage matching for broadband stability and improved gain response. This topology increases the gain per area of the circuit and for the higher bands yields a lower overall amplifier noise measure. Finally decade bandwidth is possible using a distributed amplifier design. This method is well documented in several publications [1][4][5]. In this effort however, the transistor noise parameters were included in the optimization file, and the distributed amplifier was optimized for broadband low noise performance.

During the design and layout phase critical attention was placed on producibility and testability. The design optimization includes layout parasitics, and actual measured spiral inductor performance data. This corrected for commercial CAD software limitations, and permitted more realistic parasitic simulation of the circuits. This rigorous analytical analysis was in large measure responsible for the first iteration success of these amplifier designs. The simulations were performed on SuperCOMPACT and on Touchstone to both verify simulator accuracy, as well as to take advantage of complimentary features in each package. Additional effort was taken to provide easy on-chip bias connections, and the layout was compatible with on-wafer RF probing techniques using Cascade 50-ohm coplanar probe tips. All the amplifiers used a standardized G-S-G input and output probe/bond pattern. Example circuit photographs and schematics are shown in figure 3, 4, and 9. Figure 3 shows the 2-7GHz single ended amplifier, the distributed amplifier is shown in figure 4 and the 5-11 GHz balanced amplifier is shown in figure 9.

Fabrication Much of the experience with super low noise HEMT devices is based on fabrication technology developed for discrete devices[3]. This effort used the discrete device process as the base-line and developed a MMIC compatible process for HEMTs. The HEMT structure is shown in figure 5. The GaAs HEMT material used was grown in a Varian Generation II MBE machine on a semi-insulating GaAs substrate. The layer structure grown consisted of an undoped superlattice buffer, followed by an undoped AlGaAs spacer and an n+ AlGaAs donor layer that was graded up to an n+ GaAs cap layer. The n+ GaAs cap helped minimize ohmic contact and parasitic series source resistance. The GaAlAs/GaAs superlattice structure is employed to reduce bulk substrate impurities in the HEMT structure, and to better confine the carriers in the HEMT potential well, thus reducing

Figure 3: 2-7 GHz Single Ended Amplifier
Layout and Schematic



Chip Size: 2590um X 1550um

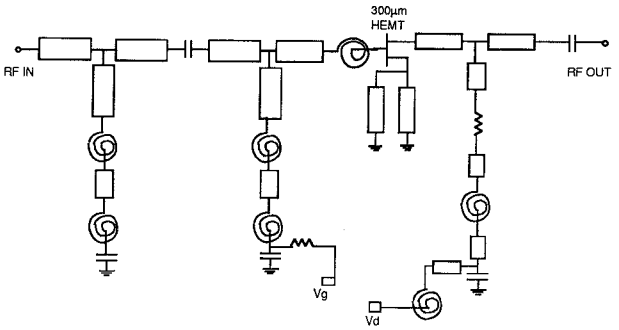
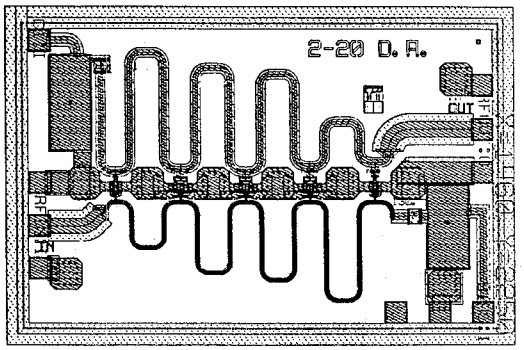
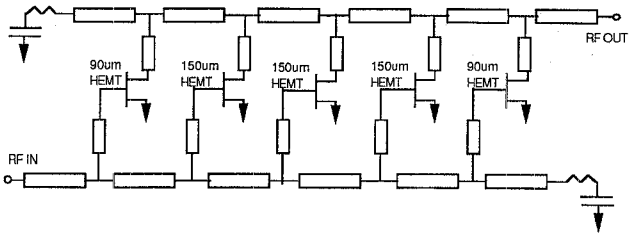


Figure 4: 2-20 GHz Distributed Amplifier
Layout and Shematic



Chip Size: 2250um x 1460um



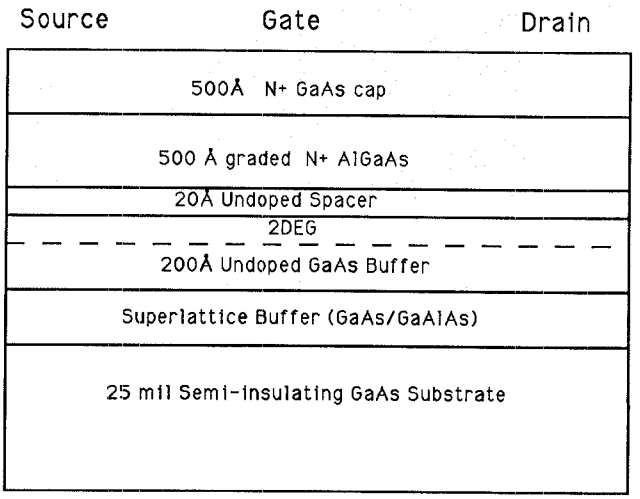
parasitic buffer current that can result from the use of submicrometer (0.2um) gate lengths. This improves the drain or output conductance and minimizes potential short channel effects.

Device isolation was acheived by using an oxygen implant. Ohmic contact was formed using a Ni-AuGe metalization that was rapid thermal alloyed. The gates are 0.2um T-gates formed using a Philips EBL system and a triple layer resist process. The HEMT MMIC additional process steps included 100 ohm per square nichrome thin film resistors, air bridge interconnect metal, silicon dioxide dielectric for MIM capacitors, etched thru vias, and plated back metal.

Performance Measurements were made using an on-wafer RF test station. The 50 ohm noise figure distribution at 12 GHz (for discrete devices on the wafer), is plotted on figure 6. The devices in the 50 ohm noise figure range 1.93-2.25dB correspond to a Fmin of 0.8-1.05dB at 12GHz. These devices showed a peak transconductance of 310mS/mm and a minimum noise transconductance of 270mS/mm. The histogram shows a typical Gaussian distribution, with high yield and small standard deviation.

Figure 5

HEMT STRUCTURE PROFILE



The amplifiers were co-located on the same wafer. All the amplifiers correlated well with predicted performance data, and thus validated the design methodology. A detailed measured versus modeled plot of the 2-7 GHz band single-ended amplifier is shown in figure 7. Note the well predicted behavior of the gain and noise figure. The transconductance for the device in this particular circuit is 150mS/mm. Input VSWR is less than 7:1 and output VSWR is less than 1.5:1. Two of these single-ended circuits are designed to be balanced in off chip Lange couplers.

Measured versus modeled data for the distributed amplifier is shown in figure 8. Note the noise figure of less than 3.5dB over the 2-20 GHz band. This is the best reported noise figure for this band to date. The input and output VSWR for the distributed amplifier is less than 1.5:1 over the 2-20 GHz band, and the IP3 is greater than 16dBm. The measured and modeled gain and noise figure for the 5-11 GHz balanced LNA is shown in figure 9.

Figure 7:

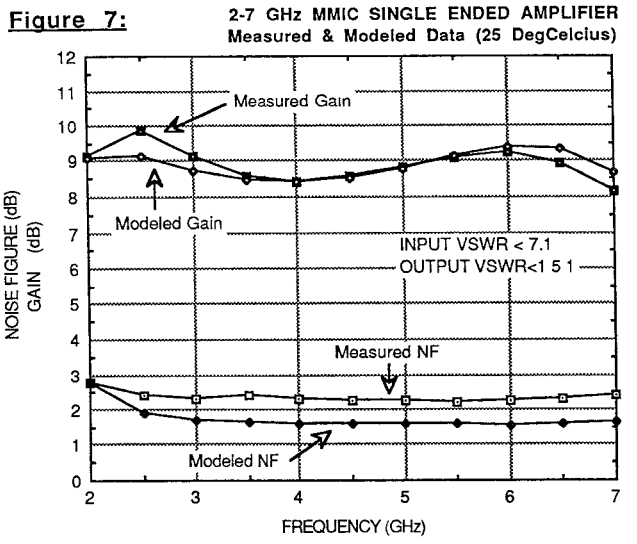
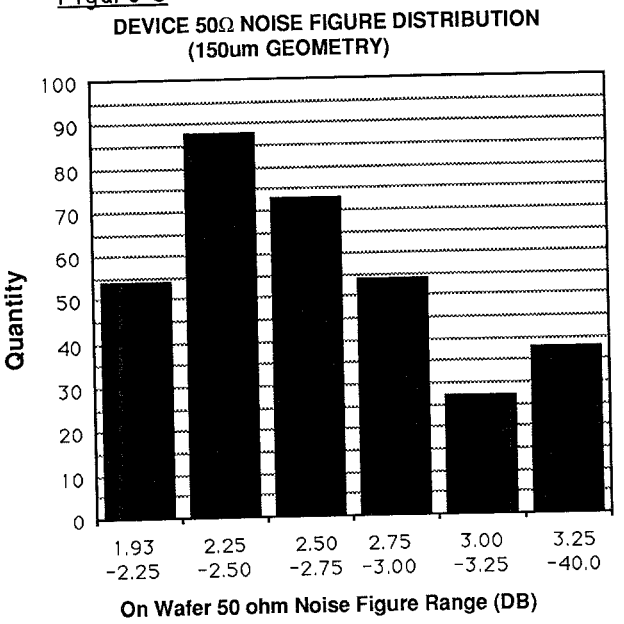


Figure 6

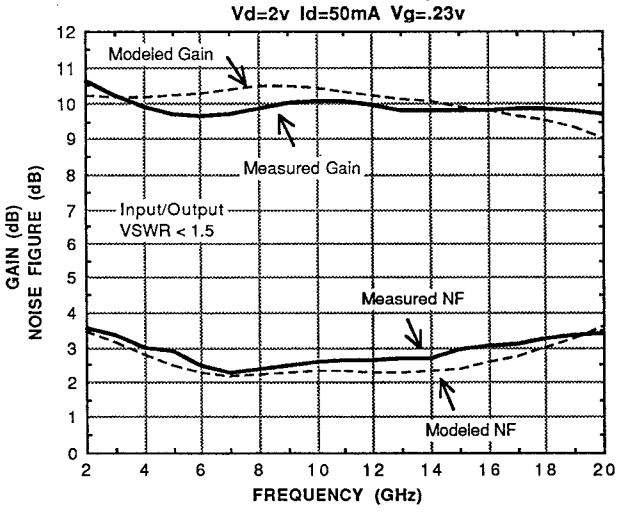


Over the 6-11 GHz band the noise figure is less than 2.5dB and the input/output VSWR is less than 2:1.

An early evaluation of the unpassivated transistor reliability was also performed. A temperature step-stress test was performed, and the HEMT devices were exposed to 200° C, 225°C, and 250°C under static bias conditions. The preliminary data was analyzed and an extrapolated MTTF of 2x10e6 hours at 100 degrees Celsius channel temperature was determined. This proves the initial high reliability of the discrete device process, and is a stable building block for future work in HEMT MMIC process reliability.

Conclusion This effort has developed a design methodology which has proven successful HEMT monolithic low noise amplifiers. The amplifiers performed as predicted, and achieved a very high process yield. A 2-7 GHz singled ended amplifier and a 5-11GHz amplifier have acheived < 2.5dB noise figure and the 2-20 GHz distributed amp has acheived 9.5dB gain with less than 3.5 dB noise figure. The performance acheived demonstrates the advances in design and processing that have taken place in analytical low noise amplifier design. Initial device reliability studies also indicate that the process is inherently stable, and capable of qualification for high reliability space applications. The tremendous advantages afforded by the availability, small size and light weight monolithic low noise amplifiers offers greater flexibility in designing future wideband front-end electronics systems.

Figure 8: 2-20GHz T-Gate HEMT Distributed Amplifier Measured & Modeled Data (25 Deg Celcius) Vd=2v Id=50mA Vg=.23v



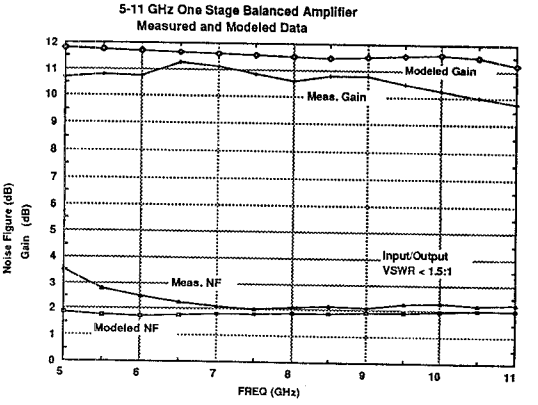
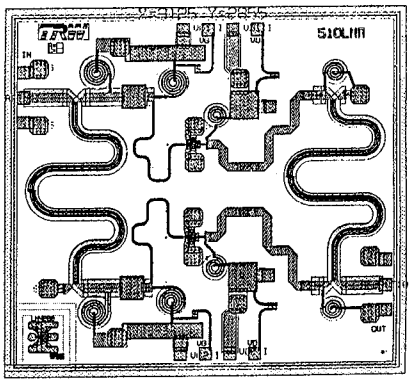
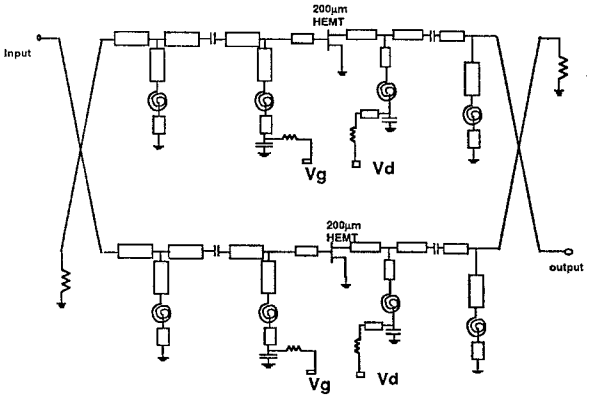


Figure 9: 5-11 GHz Balanced LNA Layout, Schematic and Data



Chip Size: 3160um x 2900um



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[1] S. Bandy, C. Nishmoto, et al., "A 2-20GHz High- Gain Monolithic HEMT Distributed Amplifier, "1987 IEEE MTT-S Int'l Microwave Symposium., pp. 155-158, June, 1987.

[2] C.A. Liechti, L. Tillman, "Design and Performance of Microwave Amplifiers with GaAs Schottky-Gate Field Effect Transistors" May 1974 IEEE Trans. MTT vol. MTT-22 pp. 510-517.

[3] W. L. Jones, S. K. Ageno, T. Y. Sato, "Very Low Noise HEMT's Using a 0.2um T-Gate" Electronics Letters, 30th July 1987, vol. 23, no.16, pp 844-845.

[4] C. Yuen, C. Nishimoto, et al., " A Monolithic 3 to 40 GHz HEMT Distributed Amplifier" Nov. 1988 GaAs IC Symposium Digest., pp105-108.

[5] P. Gamand, A Deswarte, et al., "2 to 42 GHz Flat Gain Monolithic HEMT Distributed Amplfiers" Nov. 1988 GaAs IC Symposium Digest., pp109-111.